ABSTRACT

A method is provided for forming a non-volatile memory device. The method includes forming a stacked structure including a tunnel oxide layer, a floating gate, a thin oxide layer, and a control gate on a semiconductor substrate. Etching is used to define the sidewalls of the stacked structure. Dopants are implanted into exposed areas of the substrate to form source and drain regions within the substrate adjacent to the stacked structure. A liner dielectric layer is formed on the sidewalls of the stacked structure to patch the etching damage. Thereafter, a nitride barrier layer is formed on the liner dielectric layer, and an oxide spacer is formed on the nitride barrier layer. The nitride barrier layer can trap negative charge and thus act as a relatively high barrier at the tunneling oxide edge. Therefore, the threshold voltage difference between the initial erase of the memory device and the erase after many cycles is reduced.